Prototyping using FPGAs in VLSI design

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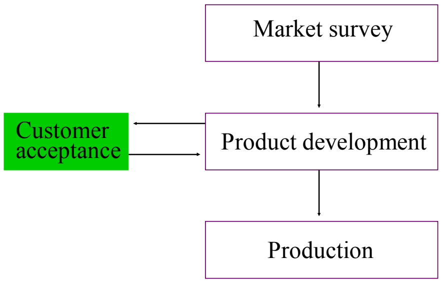
Agenda

- Why FPGA Prototyping
- How Prototyping is done
- What is achieved with prototyping

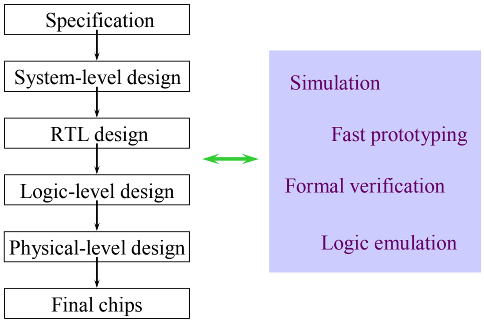
Why All Asics Should Be Prototyped??

Introduction to FPGA Prototyping

Product Development Cycle



Design Process



The problem

- Complexity of ASICs is increasing
- Time-to-Market is coming down
- Software simulation of design is slow
  - Simulation speeds are of the order of few Hz
  - Portion of whole design only can be fully verified
- Some form of hardware-assisted verification is needed

Methods

- Acceleration
- Emulation
- FPGA prototyping

Acceleration

- Involve arrays of special-purpose processor chips or FPGAs
- Simply geared to speeding the simulation of the ASIC in isolation
- Disadvantages
  - Verification does not verify the device in the context of the system
  - Very expensive
  - Accessed by only one (or very few) developers at a time

Emulation

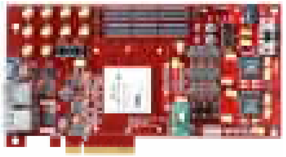
- Involve arrays of special-purpose processor chips or FPGAs
- Integrated into the system-level environment
- Disadvantages
  - Speeds in the order of only 1 MHz
  - Very expensive
  - Accessed by only one (or very few) developers at a time

FPGA prototyping

- Create a hardware model of the ASIC design
- Verify the design “at-speed”
- Real-time simulation speeds in the order of 10 MHz to 80 MHz
- Inexpensive, thereby allowing them to be provided to multiple developers

Single FPGA prototypes

- 1/3 of today’s ASIC designs are verified by means of an FPGA-based prototype
- 2/3 of the designs can be modeled using a single FPGA
- Development boards are available off-the-shelf



Issues with prototyping

- HDL code compatibility
  - Code incompatibility between the ASIC and FPGA domains like clock gating etc
- Visibility into the design
  - For ex, tools like ChipScope

Multi-FPGA prototypes

- Hardware prototype of larger ASIC designs
- Account for 1/3 of all FPGA-based prototypes
- Off-the-shelf or custom boards

Issues

- Same problems as Single FPGA prototypes
- Partitioning of design
- Synchronization of FPGA signals
- Area and timing issues
- Pin locking etc..

How prototyping is done??

ASIC Prototyping Using Off-the-Shelf FPGA Boards

ASIC Prototyping Using Off-the-Shelf FPGA Boards

- Initial designs were prototyped on custom FPGA boards
- Today there is a thriving community of off-the-shelf multi-FPGA prototyping board vendors
- Off-the-shelf multi-FPGA prototyping board industry has grown to be three-quarters the size of the hardware emulation market

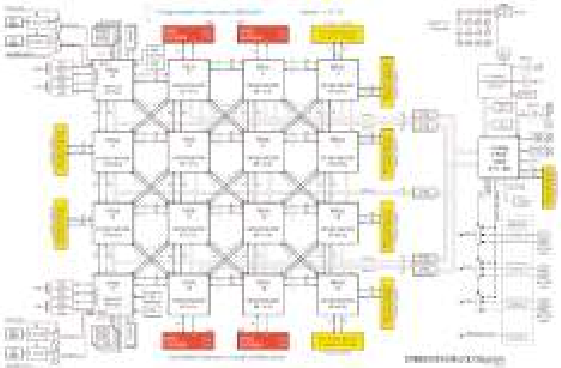
Parameters

- Better performance
  - For boards with 2-3 FPGAs custom boards never out perform commercial boards
- Ease of creation
  - For single FPGA, custom boards are easy to design
  - For multi FPGA boards, complexity increases exponentially
- Ease of interfacing
  - Interfacing is taken care by manufacturer in case of multi FPGA boards

Parameters (contd.)

- Reducing costs
  - Off-the-shelf boards are cheaper
  - No board design cost
- Reducing time-to-market
  - FPGA board making time is approx. 9 months which is saved for off-the-shelf counter parts

Typical Example



Partitioning the design

- Manual partitioning
  - Designer has better idea of how to partition
  - Grouping the design according to functionality
  - Partitioning according to timing needs
  - Synchronization may be lost if proper care is not taken
  - Area and I/O utilization
  - Keeping track of connectivity is very difficult

Automatic partitioning

- Automatic partitioning by software tools
  - Faster design partitioning
  - Some manual intervention is required for better efficiency
  - Ex. Certify

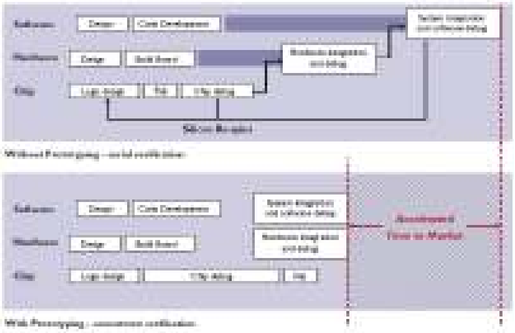
What is achieved through prototyping?

Verifying Complex ASICs through FPGA-based Prototyping

Why Prototype or Estimate

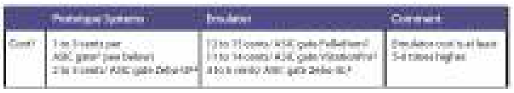
- Designs be verified and validated comprehensively prior to tapeout
- Verifying large processors such as IBM's 64-bit PowerPC used in Microsoft's Xbox, requires verification with real time devices
- Hardware-based verification alone can provide the real-time speed and interface for hardware debug
- Run software prior to the arrival of silicon

Verification phases



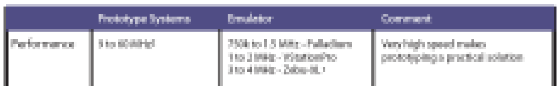
Prototype vs Emulator - Issues

1. Cost



	Prototype Systems	Emulator	Comment
Cost	1 to 3 cents per ASIC gate (see below) 2 to 3 cents/ ASIC gate Zebu-XP	12 to 15 cents/ ASIC gate Palladium 11 to 14 cents/ ASIC gate VStationPro 4 to 6 cents/ ASIC gate Zebu-XL	Emulator cost is at least 5-6 times higher

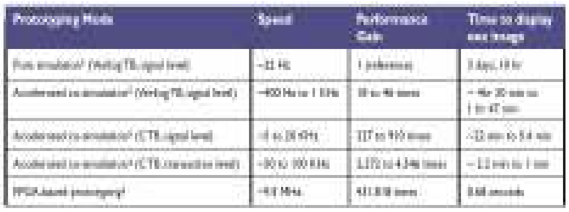
2. Performance



	Prototype Systems	Emulator	Comment
Performance	5 to 60 MHz	750k to 1.5 MHz - Palladium 1 to 2 MHz - VStationPro 3 to 4 MHz - Zebu-XL	Very high speed makes prototyping a practical solution

An example

- Below are results for a video processing chip



Prototyping Mode	Speed	Performance Gain	Time to display one image
Pure simulation (Verilog RTL signal level)	~11 Hz	1 (reference)	3 days, 19 hr
Accelerated co-simulation (Verilog RTL signal level)	~400 Hz to 1 KHz	38 to 48 times	~4hr 20 min to 1 hr 47 min
Accelerated co-simulation (C/TB signal level)	~1 to 20 KHz	117 to 910 times	~32 min to 5.4 min
Accelerated co-simulation (C/TB transaction level)	~30 to 100 KHz	3,172 to 4,346 times	~1.2 min to 1 min
FPGA-based prototyping	~4.5 MHz	431,818 times	0.68 seconds

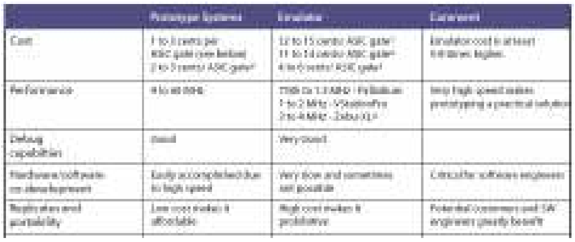
Issues (contd.)

3. Hardware software co-verification
4. System replicates
5. Debug capabilities
   - Emulator provides better debug features
   - Tools like ChipScope are useful in debugging on prototype
6. Design partitioning
7. Rate adapters
   - Required for emulator due to speed difference
8. Compile, place & route and download times

Issues (contd.)

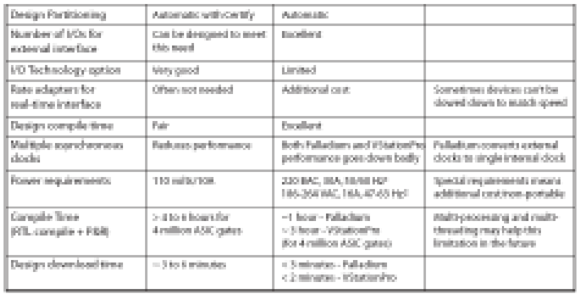
9. Power consumption
   - Emulators consume huge amount of power
   - Maintenance cost for cooling, power etc
10. I/O availability
11. I/O pin technology

Prototype or Emulator

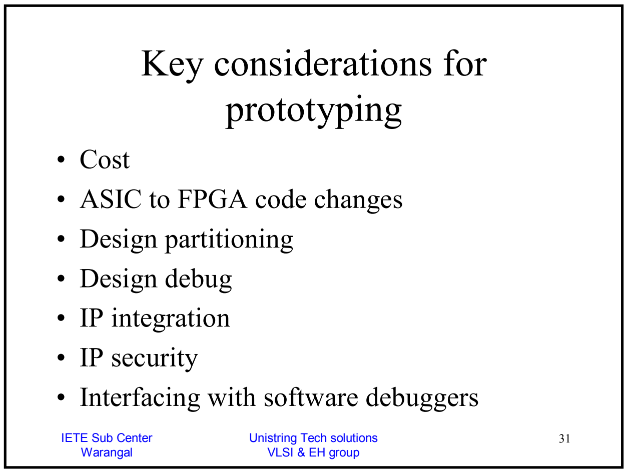


	Prototype Systems	Emulator	Comment
Cost	1 to 3 cents per ASIC gate (see below) 2 to 5 cents/ ASIC gate	12 to 15 cents/ ASIC gate 11 to 14 cents/ ASIC gate 4 to 6 cents/ ASIC gate	Emulator cost is at least 5-6 times higher.
Performance	8 to 60 MHz	750k to 1.5 MHz - Palladium 1 to 2 MHz - VStationPro 3 to 4 MHz - Zebu-XL	Very high speed makes prototyping a practical solution
Debug capabilities	Good	Very Good	
Hardware/software co-development	Easily accomplished due to high speed	Very slow and sometimes not possible	Critical for software engineers
Replicates and portability	Low cost makes it affordable	High cost makes it prohibitive	Potential customers and SW engineers greatly benefit

Prototype or emulator

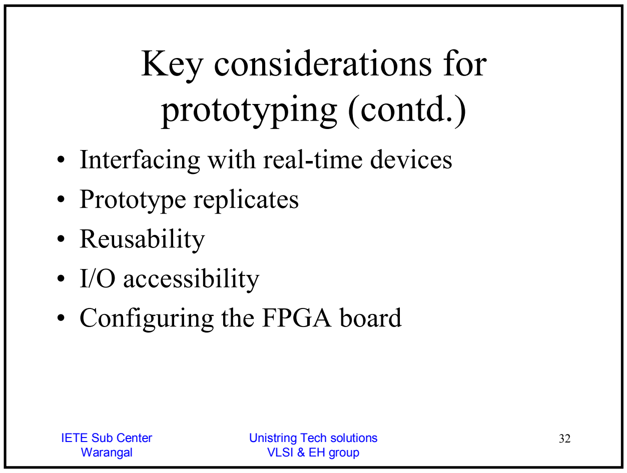


Design Partitioning	Automatic with certify	Automatic	
Number of I/Os for external interface	Can be designed to meet this need	Excellent	
I/O Technology option	Very good	Limited	
Rate adapters for real-time interface	Often not needed	Additional cost	Sometimes devices can't be slowed down to match speed
Design compile time	Fair	Excellent	
Multiple asynchronous clocks	Reduces performance	Both Palladium and VStationPro performance goes down badly	Palladium converts external clocks to single internal clock
Power requirements	110 volts/10A	220 VAC, 30A, 50/60 Hz 180-264 VAC, 16A, 47-63 Hz	Special requirements means additional cost/non-portable
Compile Time (RTL compile + P&R)	> 4 to 6 hours for 4 million ASIC gates	~1 hour – Palladium ~3 hour – VStationPro (for 4 million ASIC gates)	Multi-processing and multi-threading may help this limitation in the future
Design download time	~3 to 6 minutes	< 3 minutes - Palladium < 2 minutes - VStationPro	



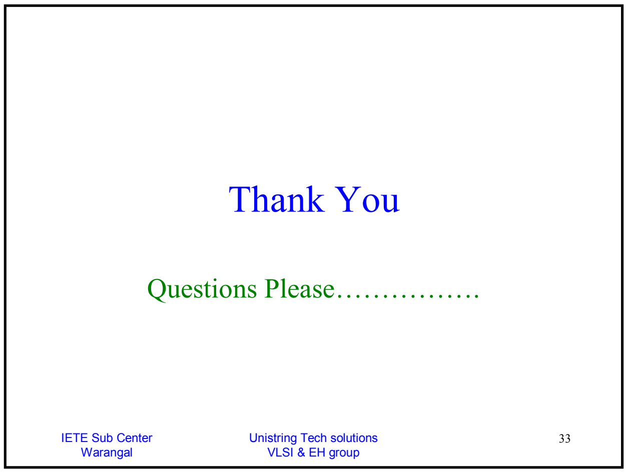
Key considerations for prototyping

- Cost
- ASIC to FPGA code changes
- Design partitioning
- Design debug
- IP integration
- IP security
- Interfacing with software debuggers



Key considerations for prototyping (contd.)

- Interfacing with real-time devices
- Prototype replicates
- Reusability
- I/O accessibility
- Configuring the FPGA board



Thank You

Questions Please…………….